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(54) Improvements in or relating to video display systems.

(57) A video display system suitable for use in video games includes a store for storing information to be displayed, a video controller for selecting from the store a plurality of dots on a raster scan display on which the information is obtained from the store after passing a parallel to serial converter to provide data on each dot sequentially to the raster scan display.

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Croydon Printing Company Ltd.

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EUROPEAN SEARCH REPORT

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EP 83 30 0104

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl ³)
A	WESCON CONFERENCE RECORD, vol. 25, September 1981, pages 1-10(31/5), El Segundo, CA, US; J.L. WISE et al.: "Color graphics with an advanced LSI controller" * Page 9, left-hand column, lines 1-24 *	1,2,5	G 09 G 1/16 G 09 G 1/28
A	ELECTRONIQUE INDUSTRIELLE, no. 21, October 1981, pages 33-36, Paris, FR; Ph. LAMBINET: "Réalisation d'un terminal graphique autour du processeur intégré EF 9365" * Page 34, right-hand column, lignes 2-7 *	1	

TECHNICAL FIELDS SEARCHED (Int Cl ³)

G 09 G 1/16
G 09 G 1/28

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-09-1985	SIX G.E.E.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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(12) # EUROPEAN PATENT APPLICATION

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(54) **Improvements in or relating to video display systems.**

(57) A video display system suitable for use in video games includes a store for storing information to be displayed, a video controller for selecting from the store a plurality of dots on a raster scan display on which the information is obtained from the store is passed to a parallel to serial converter to provide data on each dot sequentially to the raster scan display.

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IMPROVEMENTS IN OR RELATING TO VIDEO DISPLAY SYSTEMS

The present invention relates to video display systems and more particularly but not exclusively to video displays for amusement or games.

Previously known systems have used a number of shapes which are stored in a memory and displayed at locations on the screen dictated by a programme sequence. This produces a "jerky" picture when displaying moving objects and also constrains the colour used to areas dictated by the shapes. There are also known colour graphics hardware systems which are capable of displaying a 512 x 512 dot matrix of colour dots (pixels) which can be individually dot addressed. However, such systems are exceedingly complex, bulky and expensive.

It is an object of the present invention to provide an improved video display system which provides greater detail in the displayed information or picture and/or which can be less complex, bulky and expensive than known systems.

Accordingly the present invention provides a video display system including storage means for storing data to be displayed, a raster scan display for display of the data,

a video controller for selection in a single clock pulse period, the addresses in said storage means of a plurality of dots to be displayed on said raster scan display at positions determined by said video controller, and including a parallel to serial converter to provide data on each dot sequentially to the raster scan display.

Preferably the colour information is transferred during one part of each clock pulse cycle the other part of the clock pulse cycle being allowed for access to the system by microprocessor control means.

In preferred embodiments the number of dots to be displayed in each plurality is four or eight.

According to the present invention there is also provided

a method of displaying video data on a raster scan cathode ray tube including storing the video data in a digital form in a random access memory, transferring the digital video data from said random access memory to a video memory, in which a display is stored as a series of colour numbers corresponding to dots on the raster scan cathode ray tube, under the control of a programme sequence stored in said random access memory, such that the video colour data stored in said video memory is accessible under the control of a video controller to be output to a plurality of colour look up random access memories which control digital to analogue circuits for display of the video data on the cathode ray tube.

Embodiments of the present invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 shows in block diagrammatic form the control circuitry for a video display system according to the present invenntion;

Figure 2 shows the system of Figure 1 in greater detail;

Figure 3 shows a time sequence for a typical display;

Figure 4 shows a flow diagram for a typical display;

Figure 5 shows a flow diagram for achieving a colour change; and

Figure 6 shows an example of a displayed symbol.

The video display system described hereinbelow is intended for use with a Raster scan cathode ray tube system and permits vector colour graphics on the screen of a Raster cathode ray tube.

Referring now to Figure 1, the control system comprises a 16 bit processor 10 which is connected to a main data bus 12 and a main address bus 14.

Connected to the data bus 12 is a video controller 16 and connected to the video controller 16 is a multiplexer 18 controlled by the clock generator 23.

The main video random access memory 20 comprising 16 x 64K (32 x 64K for higher resolution) bit RAM is connected to the multiplexer 18. A clock generator

and controlled circuit 23 is used to provide the clock signals and control signals on outputs o/p shown in greater detail in Figure 2. The outputs of the 16 RAM'S 20 are connected to four shift registers 24 which store the outputs. The output of these shift registers 24 are connected to a multiplexer 26 which multiplexes either the video data or part of the main address bus 14 onto the address lines of the three colour look-up RAMS 28, 30 and 32, depending upon whether the circuit is in display mode or colour look-up RAM update mode as determined by the programme running from the processor. The output of each colour look-up RAM is fed via respective digital to analogue converters 34, 36, 38 to the red green and blue colour guns of the video display 39 (see Figure 2). The outputs of the 16 RAMS 20 are also connected to a latch 22 which optionally includes a multiplexer/selector which can pass the video data onto the data bus 12.

Sound generation for the display is achieved using a sound generator circuit 40 connected to the main data bus 12.

The operation of the circuit will now be described in greater detail.

The fast 16 bit Processor 10 is used tc permit the video data to be moved in the shortest possible time. A slower 8 bit version is possible which moves the data more slowly. There are 4 bits to define each dot (colour), and thus one 16 bit (word) data move in fact moves 4 horizontally adjacent dots or two pixels are moved with an eight bit (byte) data move. Another version provides for each pixel to occupy 4 bits of a byte (8 bits) in the processor address map in which case two pixels are moved with each 16 bit word data move or an individual pixel is moved with a byte data move. The Processor used is the 68000 in a preferred embodiment.

Although each group of four dots are described herein as being horizontally adjacent it will be understood that they could be vertically adjacent. Whether the dots are horizontally or vertically adjacent depends upon the physical orientation of the display CRT (vertical or horizontal), the

orientation of Raster scan which drives the CRT, or the order of the address lines between the video controller 16 and the multiplexer 18 in conjunction with their interpretation by the programme running on the processor, i.e., which part of the screen the programme considers to be top/bottom and left/right.

The video controller 16 is used to generate the address of the next 4 dots to be displayed. This dot address is fed via the Multiplexer 18 to the video RAM 20 (16 off 64K dynamic RAMS). The Multiplexer 18 provides the ability to address the video RAM 20 from the Processor Address Bus 14. The 16 bits of data out from the video RAM 20 are fed into the four 4 bit shift registers 24, which are clocked in parallel to provide a 4 bit wide colour number for each individual dot. Each video RAM 20 data access by the video controller 16 provides data on 4 dots, horizontally adjacent. A version offering twice the horizontal resolution would use 32 RAM devices in the video RAM which would still be clocked into four shift registers but each shift register would now be eight bits long and be shifted at twice the rate. A version offering twice the vertical resolution could use 256K RAMS. The 4 bits defining the dot colour are fed via a Multiplexer 26 to the 16 location 12 bit wide fast colour look-up RAMS 28, 30, 32. The Address Multiplexer 26 provides the ability to address this RAM from the Processor Address Bus 14. The colour look-up RAMS 28, 30, 32, provide a look-up table to define the actual colour. The 4 bits from the video RAM 20 addressing one of 16 locations, each of which contains 12 bits of data, which are used in 3 groups of 4 to drive fast Digital to Analog Converters 34, 36, 38. In the version where each pixel uses only 4 bits from each byte in the processor address map, further bits may be used which can correspondingly increase the size of the colour look-up RAM and the number of shift registers but permit a greater number of colours to be selected i.e. 5 bits allows 32 colour locations. The output of the Digital to Analog Converters drives the red, green and blue guns of the television tube, so that for any particular colour code, each of the 3 guns can be set to 1 of 16 predetermined levels, giving 4096 possible colours.

A general purpose asynchronous character serial output is provided.

Preferably a custom chip is used for the clock generator and control circuit 23 (Uncommitted Logic Array) to generate all of the timing signals for the video RAM 20, and in addition address decoding for the programme memory, data memory and input/output circuits 44, 46, 48, 50.

Conventional EPROM or ROM Program Memory is included in RAM 42, with options for 32K bit, 64K bit or 128K bit EPROMS. A convenient linking arrangement is used, whereby all required signals are brought to a dual in-line header, and an option socket plugged onto the header determines which type of EPROM is to be configured.

The programme memory consists typically of EPROM or ROM memory chips and will contain the computer programme which is executed by the processor to control operation of the complete system. This memory contains all information to define the sequence and pattern of all accesses to the random access memory and the video memory. To change the function and application for the use of this circuit, one changes the programme memory chips. The random access memory is used as data workspace by the processor when executing the programmes from the programme memory. It is non-volatile so that when power is removed the contents of the RAM do not corrupt. The video memory is a complete dot image of the screen. To alter the displayed image, the processor, under control of the programme memory, writes to the video memory to alter information displayed. For convenience the video memory can also be read.

For the data memory a CMOS RAM 42 with battery back-up is employed. An option is available whereby, when the programme memory is placed upon a separate memory module PCB, the CMOS RAM is also placed there together with its battery back-up and circuitry for protecting the CMOS RAM from data corruption during power supply interruption and/or malicious or otherwise interference. This facility permits non-volatile data on machine performance, to be retained, even when the control unit is replaced, should it become faulty, because the programme module will remain with the equipment even if the rest of the controller has to be replaced.

The sound generator 40 operates using a fairly conventional method of sound generation utilising the General Instruments Chip AY-3-8912.

Referring now to Figure 2, a multiplexed input scheme 51, is employed, with 3 bytes, each of 8 bits, being enabled by switch common 1, 2 or 3. Steering diodes are used to separate data from one byte to the next. The switch commoned strobe and the 8 bits of input all connect to the input/output lines available on the sound generator chip 40. Alternatively the multiplexed input bytes can be gated onto the processor bus for inputs using a tri-state buffer, though in this particular application they connect via the tri-state buffers contained within the sound effects generating chip 40.

Addressable output latches 44, 46, 48, 50 are utilised, which connect directly to the Processor Address and Data Bus, providing 32 lines of output. Each output may be similar, consisting of a Darlington transistor together with at least

one, and preferably a pair, of safety catch diodes or one or more of the outputs may be changed to drive a triac.

A switching regulated power supply 52 (fig.2) is employed to generate logic rail at 5 volts, 1.5amps nominal from a 24 volts AC input. The fullwave rectified 24 volts rail, and the +24 volts DC rail, are also used to provide a feed to the loads which are connected to the outputs as described above.

A quad 2-input Schmidt trigger CMOS package 53 is used to generate a power failure detect signal and a reset signal. This CMOS package is powered permanently from the battery used for the non-volatile RAM. The input is fed from a potential divider circuit, which ensures that at the worst case power fail detect is active 10 milliseconds before reset is active, which is active 10 milliseconds before the 5 volt droops. On power up an RC timing circuit ensures that reset remains active for at least 200 milliseconds after the 5 volt rail is established. In the option with the non-volatile CMOS RAM on the PROM Memory Module, this reset/power fail detect circuit would also appear on that module, as the reset output is used to protect the RAM Chip Selects during power down conditions.

With reference to figure 2, the addresses on the address bus 14, are given the prefix A and the data lines are given the prefix D. The signals from the clock pulse generator and controller 23 are referenced and connected as indicated to the Processor and other circuits. Where not otherwise indicated connecting lines at the same level are used to indicate connection of the same signals to similar circuits. Thus in the 16 x 64K Video RAM 20 the addresses A_0 to A_8 are connected

to all of the sixteen memories.

With reference to figure 3, as an example if a display of 512 x 512 dots is envisaged then if a 400 nanosecond clock period is used then this period represents in time the period of displaying four dots horizontally on the screen. This 400 nanoseconds is split into two halves. The first half of 250 nanoseconds is not used by the video circuit and is available for the processor to access the video memory for read or write should the processor require to do so. Circuitry is embodied which provides for transparent access during this period. Hence the processor can access the video memory 50 per cent of the time, and the maximum that the processor has to wait is 200 nanoseconds. The second half of the cycle of 200 nanoseconds is always used by the video circuit to do a video access to the video memory. A memory read is performed during this period and the 16 bits read are clocked into the shift registers at the end of this period. During every 400 nanosecond cycle the shift registers are clocked four times, i.e., every 100 nanoseconds. Hence the four dots loaded in parallel at the end of the previous 400 nanosecond cycle are made available to the video circuit sequentially every 100 nanoseconds throughout the following 400 nanosecond clock period.

Thus a line of 512 dots is displayed in 51.2 μs, every 64 μ seconds giving a display time of approximately 30 milliseconds per picture of 512 lines. Although there are only 512 displayed lines, the video controller generates clocks for additional lines to ensure that the total number of lines is that of a standard line system, e.g., 625 lines. The 625 lines are

repeated every 40 milliseconds. In fact the video controller 16 interlaces alternate lines every other frame. In addition to the European standard of 625 lines 50 Hz, the video controller may also be initialised for other line systems, e.g. 525 lines 60 Hz. The access time of 200 nanoseconds is acceptable for most fast memories, latches etc., and therefor the circuit allows the display from a digital memory of information on a screen allowing individual dot discrimination. During the time available for microprocessor access in the first half of each clock cycle the microprocessor can change the information in for example the colour look up RAMS via the data lines D_0 to D_{11} on the information in the Video RAMS 20. As the video circuit utilieses the colour look-up RAMS continuously throughout the displayed area of the screen, it is necessary to synchronise updating of the colour look-up RAMS to the frame fly-back period if the display is not to be affected momentarily during one or more dots.

Though the above description has been restricted to the "parallel" display of four dots the number of dots can be varied by increasing or decreasing the number of video RAMS registers and colour look up RAMS.

The colour look up RAMS give the colour information relating to each dot at a rate of four times the clock pulse i.e., every 100 nanoseconds. Thus the D to A converters must be able to cope with this conversion rate.

In a modification of the present invention a programmable logic array 60 is inserted into the circuitry and the inputs of this array are connected for example to one or more of the outputs from the microprocessor. The outputs of the array are connected to other points in the rest of the circuitry. Thus by programming the logic array to a given array the circuit can be operated as an incription circuit which can be varied for each type of machine sold. Thus if a new game becomes available then the old machine can not be used to display the new game even if the programme for the new game is obtained from one of the new machines. To enable the old machine to display a new game it will be necessary to have both the new programme and also the new programmable logic array. Since the programmable logic array may be made from a programmable array logic it will not be possible to duplicate this without a great deal of work because if it is of the "burn in" type it will not be possible to easily determine the pattern used. An alternative could be a shift register with complex feedback paths which could be burned out to give an incripted output after say a delay of three or four clock pulse periods.

In a further practical embodiment of a display for a game it is proposed to insert a Programmable Logic Array 62 PLA between the processor 10 and the data bus 12. Thus the game programme by itself would not be intelligible unless used on the machine with the correct PLA between the processor and the data bus.

As an alternative the information in the Programme PROM

could be modified for example by inversion of every other bit and an output device which re-inverted every other bit could be used to correct the programme sequence prior to its use in the machine.

In the system described hereinbefore only 16 colours can be displayed at any one time, though from a library of 4096. This can be increased by allowing various areas of the screen to be mapped, each with its own separate colour look-up RAM. This is achieved by increasing the size of the colour look-up RAM. The additional address lines may for example be driven by a new circuit consisting of an additional multiplexer, a colour map RAM, and a D-type latch.

The two inputs to the multiplexer come respectively from the multiplexer 18 and the processor address bus, and generate an address for the colour map RAM. The colour map RAM data inputs connect to the processor data bus with the data outputs connecting through the D-type latch to the additional high order address lines of the colour look-up RAM 28, 30, 32. "Two" raised to the power of the colour map RAM width defines the number of different colour look up table available, each table having the standard number of sixteen entries. The circuit functions as follows: each area of the screen is effectively described by the address emanating from block 18 when a video read is in process. This is fed via the multiplexer to the colour map RAM, which determines which set of colours is to be used for this area of the screen. This is effected by the output of the colour map RAM generating high order address lines to the colour look-up RAMS to page from one set of 16

look-up colours to another set of 16 look-up colours.

The D-type latch ensures that transition from one to another occurs synchronously at the end of a four dot clock period. The processor has the ability to write to the colour map RAM using the address bus and data bus with the multiplexer correctly selected, and can thereby define which colour look-up tables are used on which section of the screen. One possible arrangement would be for the screen to be split up into blocks of 16 dots x 16 dots, and a location allocated in the colour map RAM for each particular block. In this way a total of 64 x 64 pages of colour look-up would be possible. Another arrangement could have a 64K by 1 bit RAM in parallel with video memory to give just two banks of tables with a total possible number of colours 32. Each 4 adjacent horizontal dots would then select one bank or the other as determined by the contents of the corresponding bit in the 64K colour map RAM. In some applications it may not be a requirement to have the colour map RAM at all in which case the output from multiplexer 26 would drive the red, green and blue lines in a binary manner.

With reference to Figure 4 a typical sequence of operation is given for a game or other display. The machine is initially switched on or reset and this initialises the video controller and then the colour map. At this stage the video data stored in memory 42 has been transferred to the video memory 20 under the control of the programme also stored in memory 42.

The display then awaits the operation of switches on the machine or if none are operated it proceeds to the next display and writes further video data into the video memory 20 from the main memory 42 as specified by the programme. The programme can take any suitable form giving a desired sequence of displays.

If the sequence of displays has finished the programme is terminated but if not then the machine may await further operations of switches on the machine.

When video data is transferred from memory 42 to video

memory 20 it is transferred to specified positions in the memory 20 as specified by the programme and by information stored in the microprocessor for example as a result of operation of switches on the machine. This enables the display of four pixels per word (16 bits) or two pixels per byte (8 bits) of data on the screen and hence gives a better picture definition than previously obtainable.

This system enables a number of effects to be obtained in a simple manner. Firstly for simulation of a reel display for a "fruit" machine a forshortening effect can be produced to give characters a fraction of the size of the centrally diplayed character to give the effect of a circular reel. For exammple if a character is stored in memory 42 to require ten lines (0 - 9) of display then normally it will be stored in memory 20 as ten lines (0 - 9).

If a half size character is required then every other line can be omitted when the character is transferred to memory 20. Thus only lines 0, 2, 4, 6, and 8 will be stored in five positions in memory 20 and thus the character will appear on the screen as half size in height. Thus it is only necessary to store full size characters in memory 42 and they can be displayed to any scale as specified by the programme or the microprocessor.

The information on colour in the video memory 20 is held as a number between one and sixteen. This number is converted by the colour look up memories and D to A converters into the displayed colour. This can be used to advantage. For example if a symbol is displayed on the screen in a variety of colours then on depression of a switch or after a time out period the colours can all be changed by the microprocessor transforming the colour numbers for that symbol in the video memory 20. As a simple case it could add one (1) to all colour numbers. Thus where a symbol was red blue and green (colour numbers 2, 3 and 4) it could become blue green and yellow (numbers 3, 4 and 5) by adding one to all the colour numbers. If done on a repetitive sequential time-out basis then the symbol will flash from one colour to another. In the same manner silhouettes can

be achieved.

A further method of altering the characters displayed is shown in Figure 5. Suppose a symbol "A" is displayed in two colours 1 and 2, then by initialising a short programme stored in memory 42 to change the colour map contents as contained in the memories 28, 30, 32 the colour of the symbol stored in video memory 20 can be changed as displayed even though its colour numbers as stored in memory 20 are not changed. The delays are built into the programme because otherwise the change of colour would occur too rapidly for the human eye to see. This technique can be used to provide flashing symbols and for example time effect colour changing pictures such as sunsets etc.

A further feature of the system is in the display of pictures with large areas of symbols which must appear to move smoothly such as for example the simulation of reels moving on a fruit machine. To provide an acceptable picture it is proposed to update only for example every second, third or fourth line for each "frame" in a cyclic manner using a software interlace technique provided by a programme stored in the memory 42. Thus it is possible to provide an update of each area of the screen where fast movement requires to be depicted. Because the area is fast moving the human eye will not notice since it expects to see a moving character and therefore does not require to focus onto it as would be the case with a stationary character. The programme can be terminated on a time-out basis when for example a reel on a fruit machine has "spun" until it comes to rest to display the symbol.

A further feature of the system is that by writing video data directly into the colour map random access memory a picture can be displayed which can switch from between four separate black and white pictures without rewriting the video data in the memory 20 which is responsible for the actual figure or number displayed. Thus a "flashing" announcement board type of display can be provided to switch between messages without updating memory 20 but merely by changing the

colour look-up map.

A further feature is the possibility of displaying a symbol on an already existing background without surrounding it with a different colour. With reference to Figure 6 the letter "A" is shown in a rectangular block as two colours 1 and 2. If colour 1 is stored as a zero colour say colour number "0" which has no colour then when the symbol block is displayed only the "A" will be displayed, the rest of the block being the colour of the background of the screen.

In an alternative arrangement each byte stored in the video memory 20 can be used to store only one pixel. In this arrangement an individual pixel can be addressed as opposed to the previously described arrangement in which with the storage of two pixels per byte it is only possible to address two pixels together and therefore four pixels per word using the 16 bit microprocessor. By not packing each byte it is easier therefore by storing for example only one pixel per byte to change one pixel on the display as a read of the packed pixels prior to modification is not required. A modified decoding circuit is required to ensure that the correct four address bits are used for addressing the single pixel within a byte or word.

CLAIMS

1. A video display system including storage means for storing data to be displayed, a raster scan display for display of the data,

a video controller for selection in a single clock pulse period, the addresses in said storage means of a plurality of dots to be displayed on said raster scan display at positions determined by said video controller, and including a parallel to serial converter to provide data on each dot sequentially to the raster scan display.

2. A video display system as claimed in Claim 1 including a fast colour look-up memory addressed by the information from the plurality of dot addresses to provide colour information for the plurality of dots to be displayed on the raster scan display.

3. A video display system as claimed in Claim 1 in which the video controller is controlled by a clock generating means which provides a clock pulse cycle in two portions, in which information from the plurality of dot addresses is transferred during the first portion of each clock pulse cycle and in which during the other portion of the clock cycle the storage means may receive data to update the display.

4. A video display system as claimed in Claim 3 including a further storage means for the storage of video information and including control means for controlling the transfer of information from said further storage means to said storage means.

5. A video display system as claimed in Claim 4 in which said control means is a microprocessor.

6. A video display system as claimed in Claim 5 in which

said microprocessor is connected to a data bus and an address bus for the receptive passage of video data and instructions throughout the system.

7. A video display system as claimed in Claim 6 including an incrypton device connected between said micro processor and said video data bus such that the information on said data bus is a combination of the instructions from the microprocessor and the incrypton such that without the correct incrypton the system will not operate.

8. A video display system as claimed in Claim 2 in which the fast colour look up memory includes additional colour information relating to selected areas of the raster scan display to change the colour in those areas relative to other areas.

9. A video display system as claimed in Claim 1 in which the plurality of dots to be displayed is four or eight.

10. A video display system as claimed in Claim 2 in which the fast colour look up memory connect digital video data into analogue quantities for the raster scan display in which they can provide an output approximately equal to the required colour.

11. A method of displaying video data on a raster scan display including storing the video data in a digital form in a random access memory, transferring the digital video data from said random access memory to a video memory, in which a display is stored as a series of colour numbers corresponding to dots on the raster scan display, under the control of a programme sequence stored in said random access memory, such that the video colour data stored in said video memory is accessible under the control of a video controller to be output to a parallel to serial converter to provide data on each dot sequentially to the raster scan display.

12. A method of displaying video data as claimed in Claim 11 including a plurality of colour look-up random access memories which control digital to analogue circuits for the display of the video data on the raster scan display.

13. A method of displaying video data as claimed in Claim 12 in which the colour look up random access memories are addressable to change the colours displayed on the cathode ray tube.

14. A method of displaying video data as claimed in Claim 11 in which the video data transferred from the random access memory to the video memory is modified to change the displayed information.

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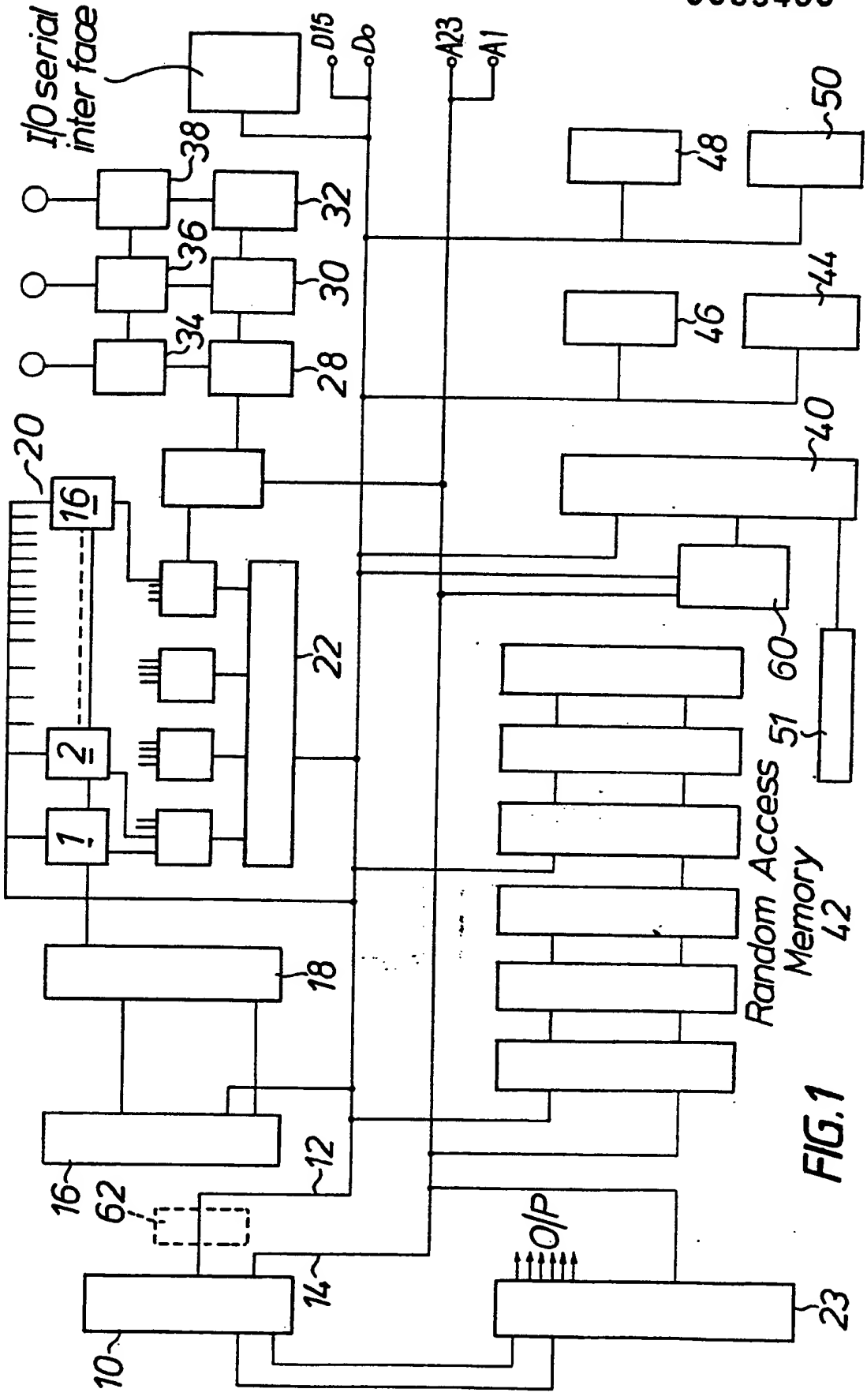


FIG.1

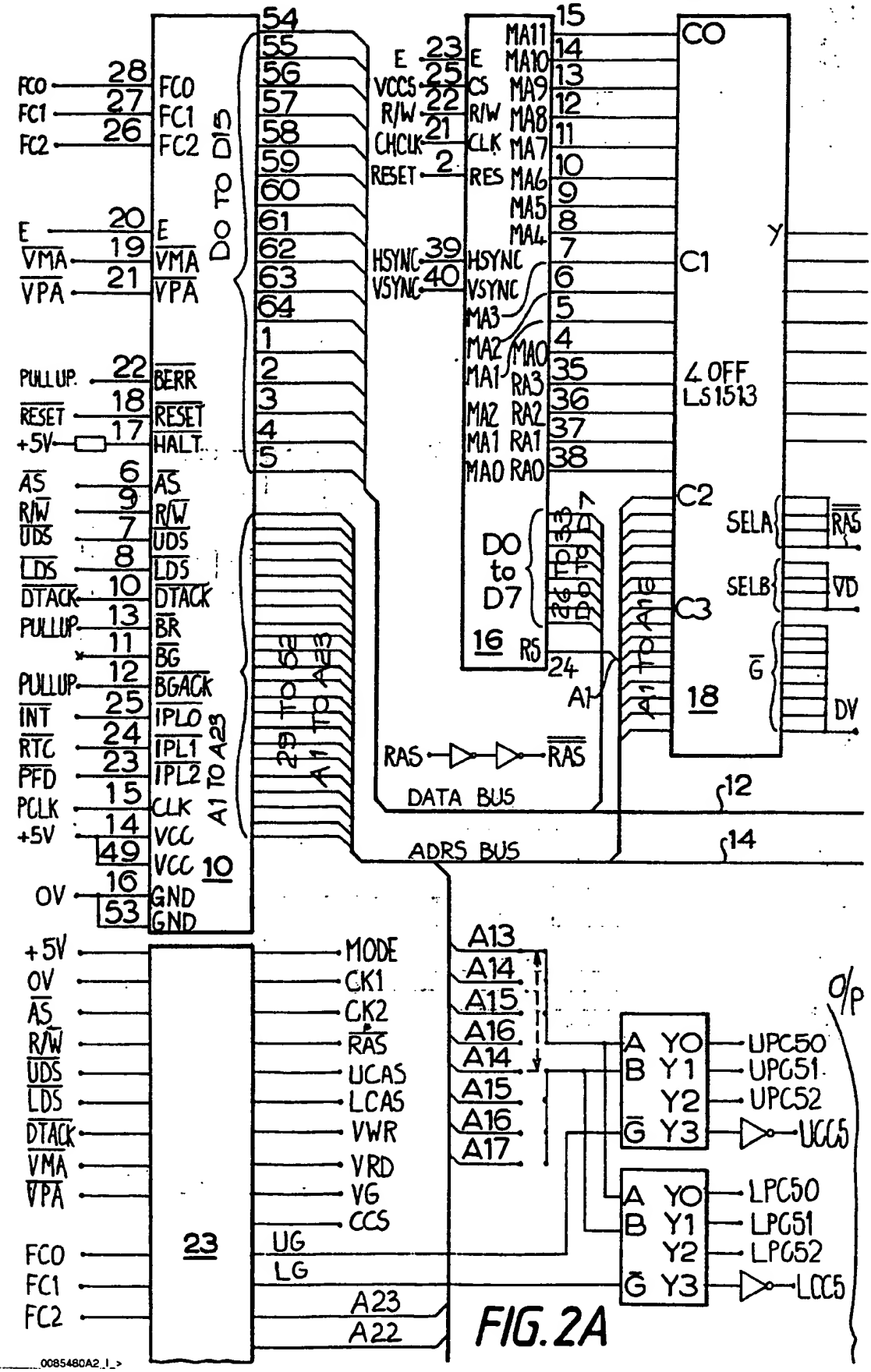


FIG. 2A

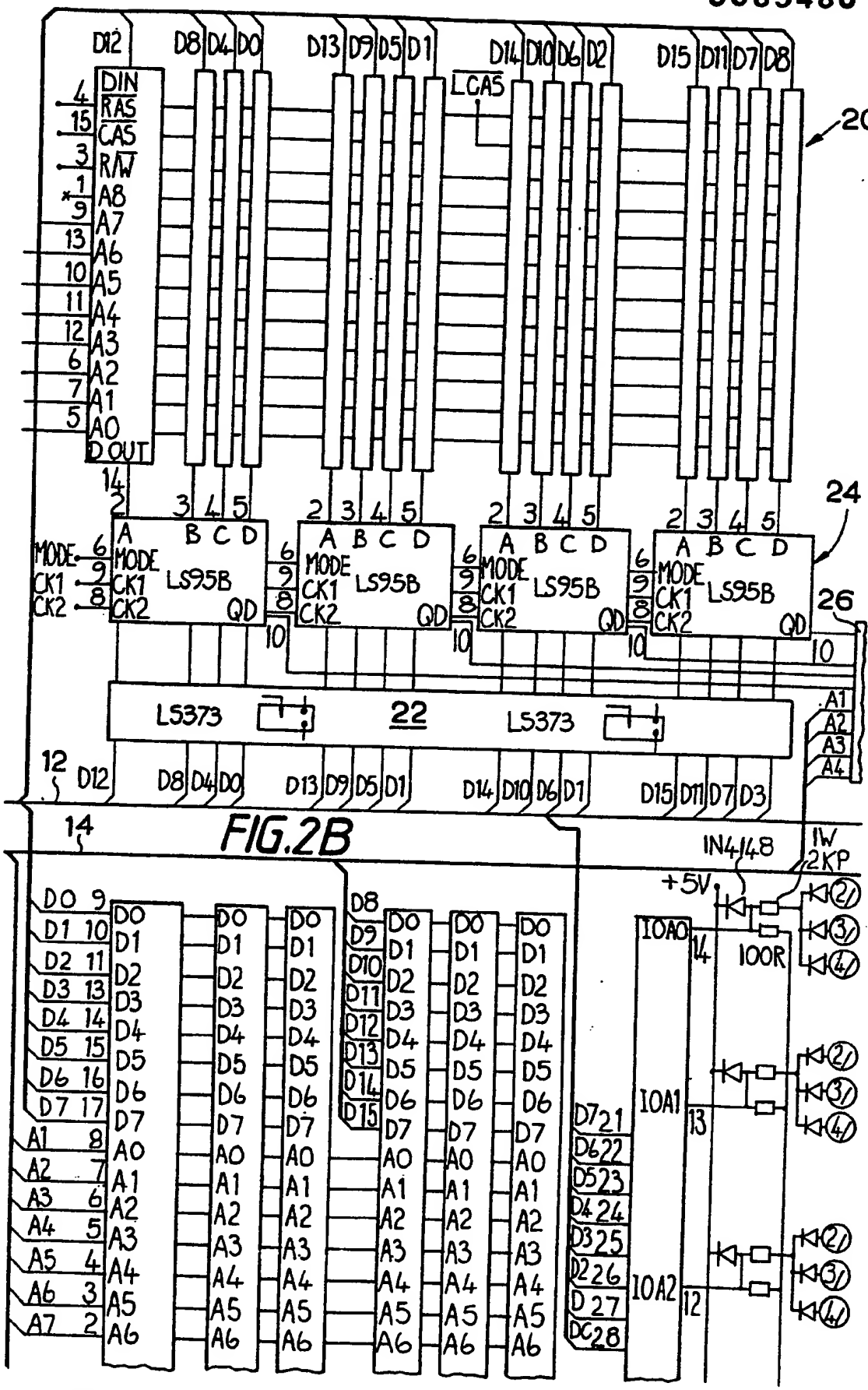
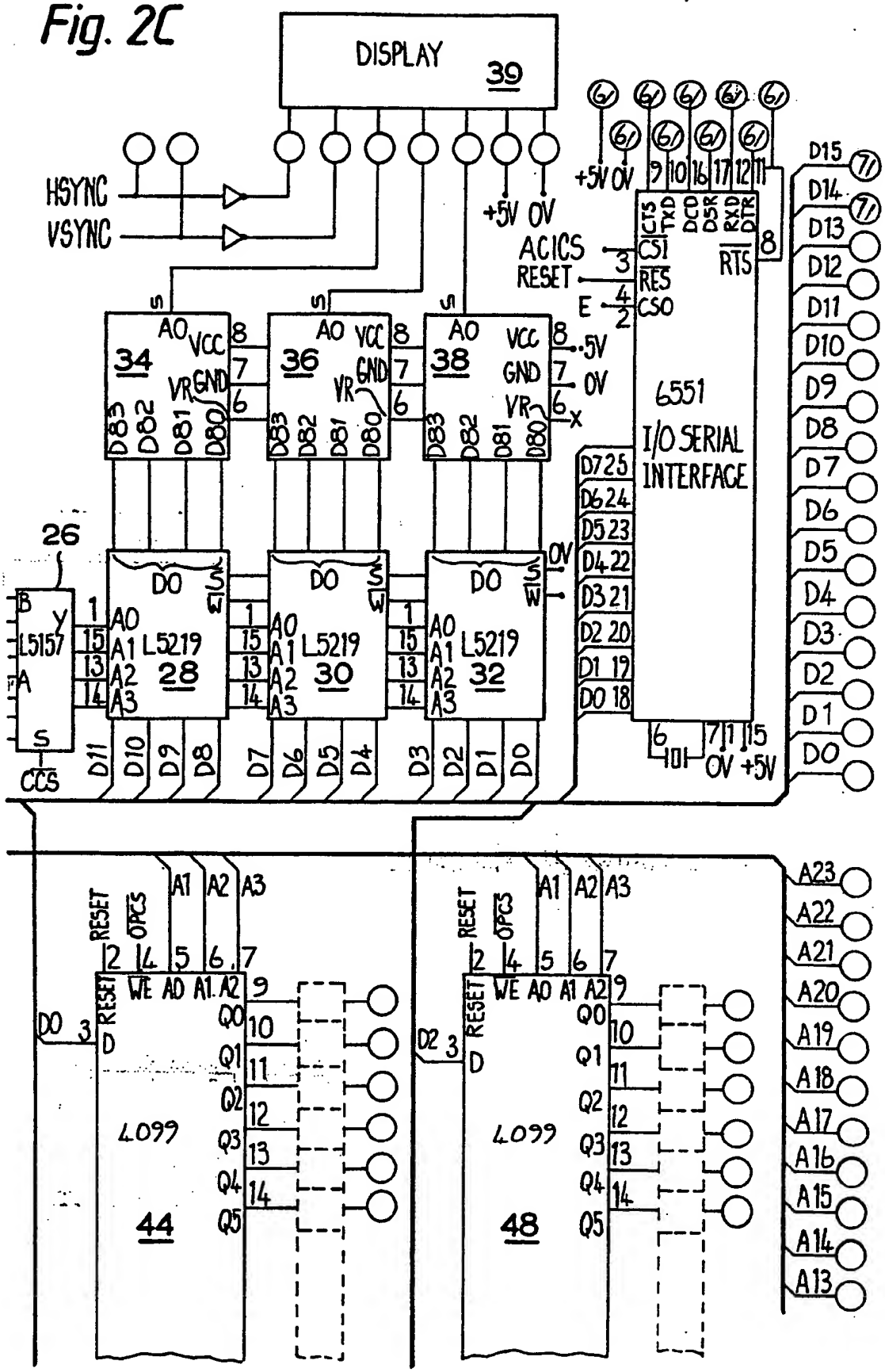

D12 D8 D4 D0 D13 D9 D5 D1 D14 D10 D6 D2 D15 D11 D7 D8
LCAS
20
DIN
RAS
CAS
R/W
A8
A7
A6
A5
A4
A3
A2
A1
A0
DOUT
24
MODE
CK1
CK2
LS95B
QD
26
L5373
22
IN4148
1W
2KP
+5V
100R
IOA0
IOA1
IOA2
D7 D6 D5 D4 D3 D2 D
DO D1 D2 D3 D4 D5 D6 D7 A1 A2 A3 A4 A5 A6 A7

FIG.2B

Fig. 2C



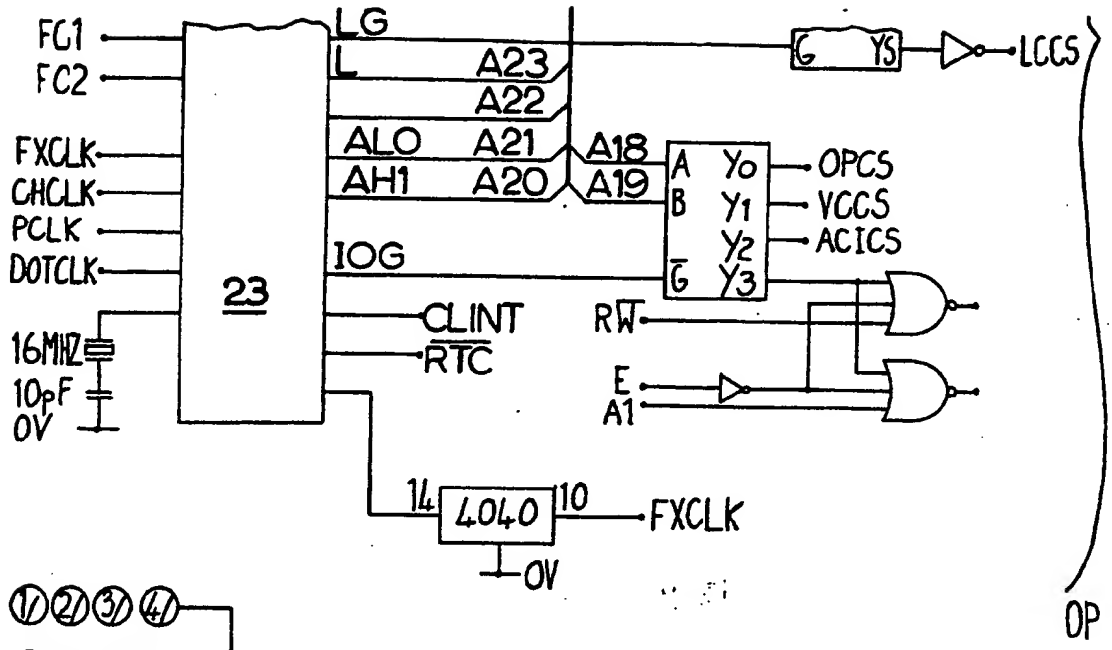
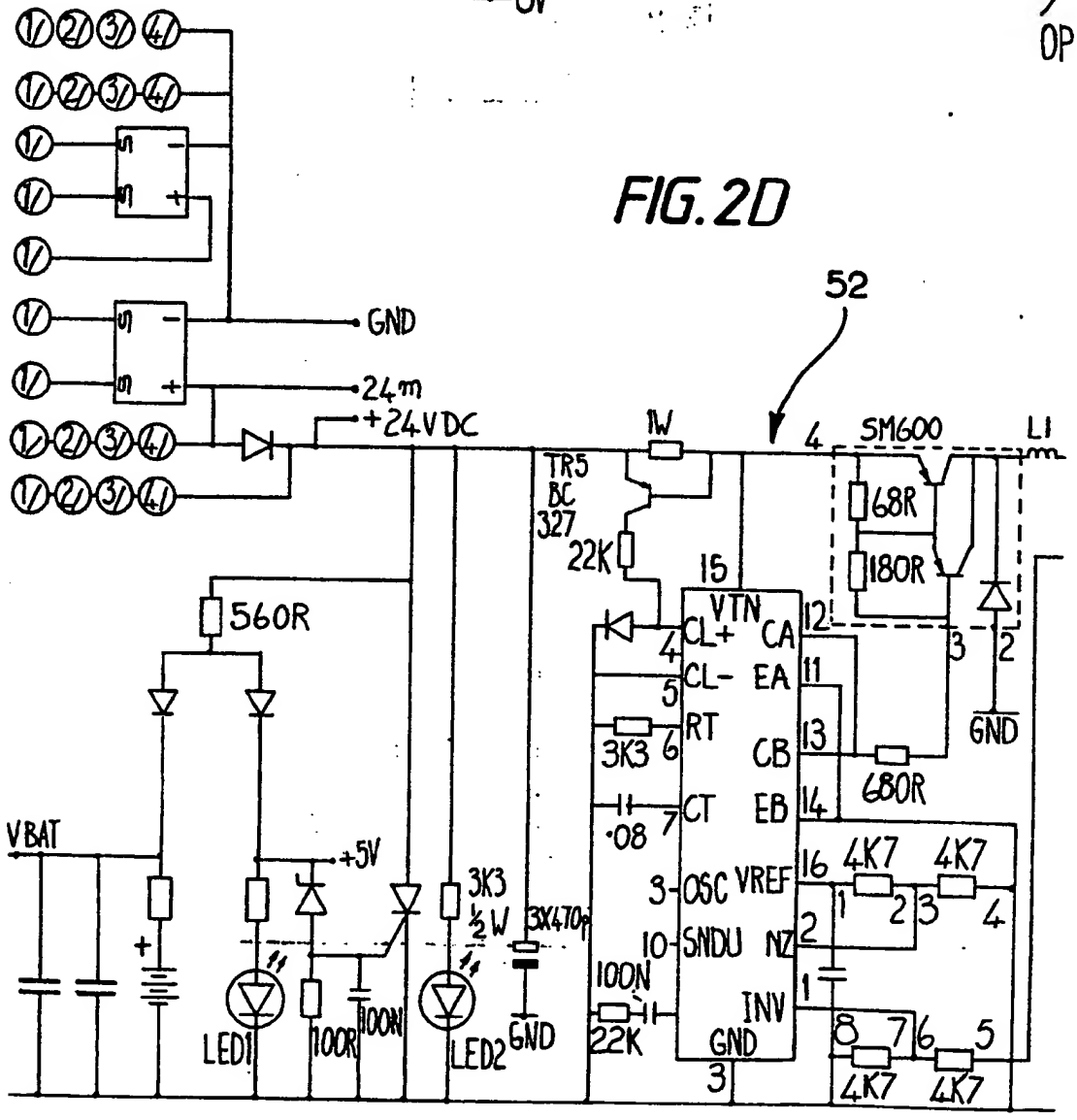

FC1
FC2
FXCLK
CHCLK
PCLK
DOTCLK
16MHZ
10pF
0V
23
LG
L
A23
A22
ALO
A21
AH1
A20
IOG
CLINT
RTC
A18
A19
A
B
G
Yo
Y1
Y2
Y3
OPCS
VCCS
ACICS
RW
E
A1
G
YS
LCCS
14
4040
10
FXCLK
0V
OP

FIG. 2D


GND
24m
+24VDC
52
1W
4
SM600
LI
TR5
BC
327
22K
68R
180R
15
VTN
CL+
CA
CL-
EA
RT
CB
CT
EB
OSC
VREF
SNDU
NZ
INV
GND
12
11
13
14
16
1
2
3
10
8
7
6
5
3K3
.08
100N
22K
680R
4K7
560R
VBAT
+5V
3K3
½W
3X470p
LED1
LED2
100R
100N
GND

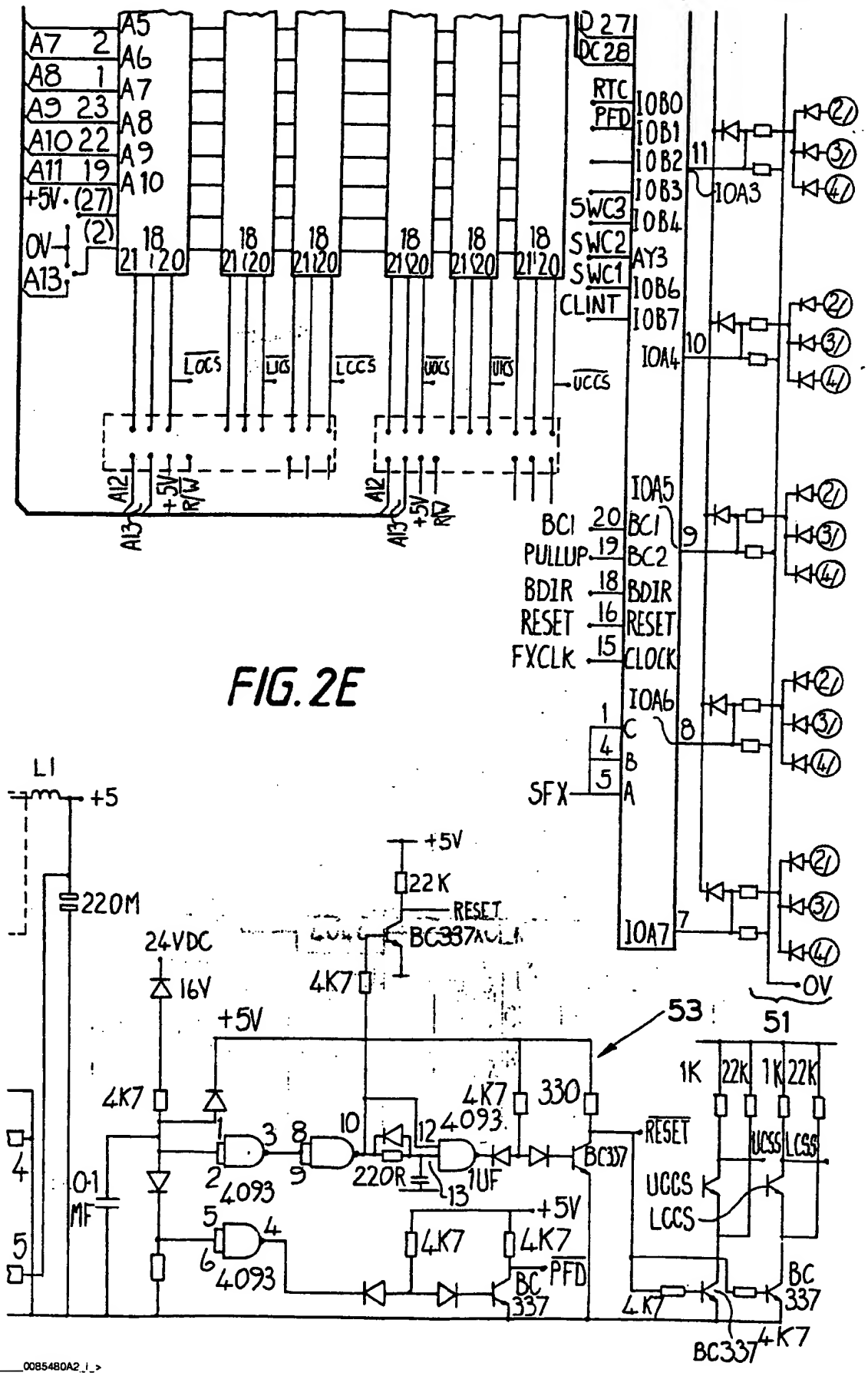

A7 2
A8 1
A9 23
A10 22
A11 19
+5V (27)
0V (2)
A13
A5
A6
A7
A8
A9
A10
18
21 20
LOCS
LUCS
LCCS
UOCS
UUCS
UCCS
A12
+5V
R/W
D 27
DC 28
RTC
PFD
SWC3
SWC2
SWC1
CLINT
IOB0
IOB1
IOB2
IOB3
IOB4
AY3
IOB6
IOB7
IOA3
IOA4
IOA5
IOA6
IOA7
BC1
PULLUP
BDIR
RESET
FXCLK
BC2
CLOCK
SFX
A
B
C
L1
+5
220M
24VDC
16V
22K
4K7
BC337
0V
53
51
330
4093
220R
1UF
0·1 MF
1K
22K
UCCS
LCCS
BC 337
PFD

FIG. 2E

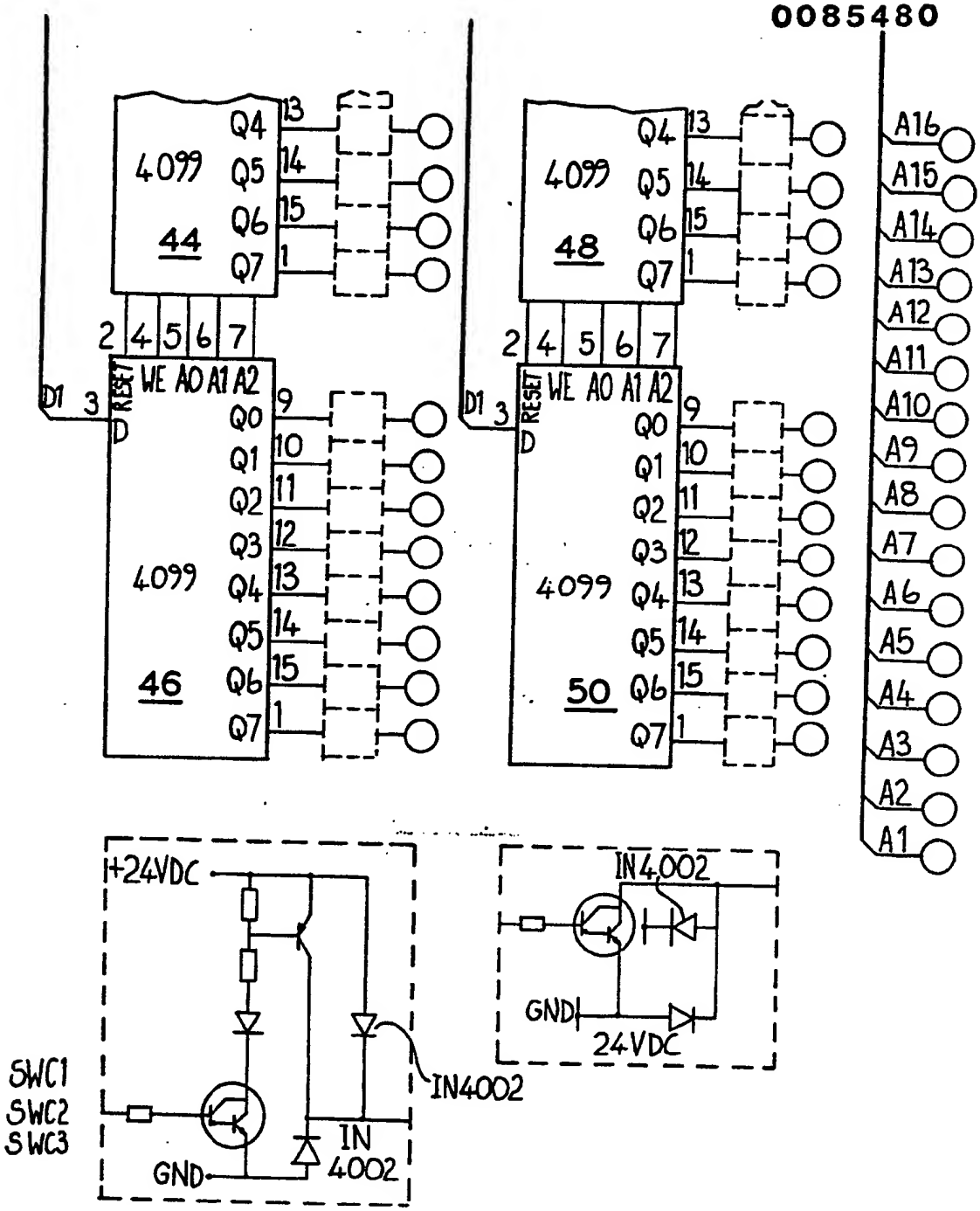

4099
44
Q4
Q5
Q6
Q7
13
14
15
1
2 4 5 6 7
D1 3
RESET
WE AO A1 A2
4099
46
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
9
10
11
12
13
14
15
1
4099
48
4099
50
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
+24VDC
SWC1
SWC2
SWC3
GND
IN
4002
IN4002
IN4002
GND
24VDC

Fig. 2F

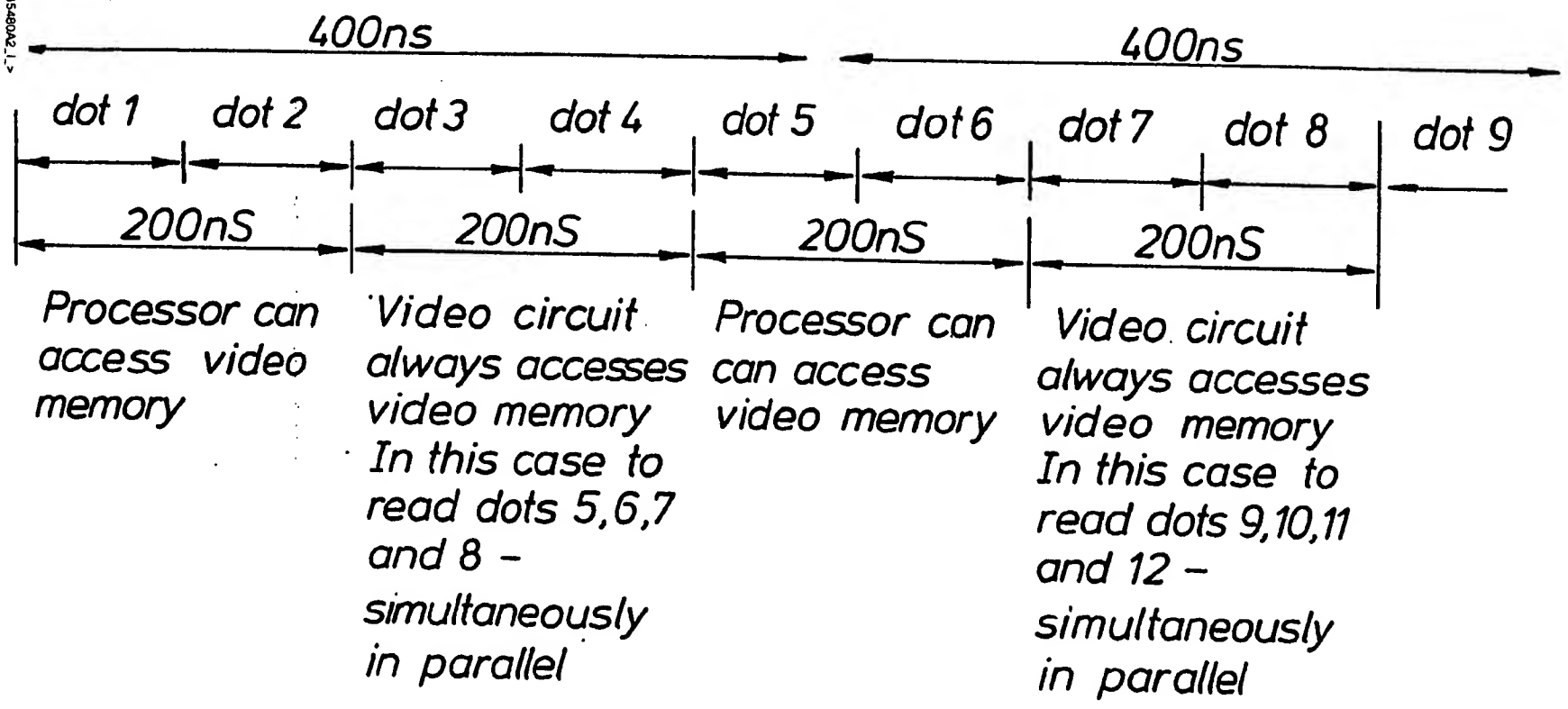


FIG.3

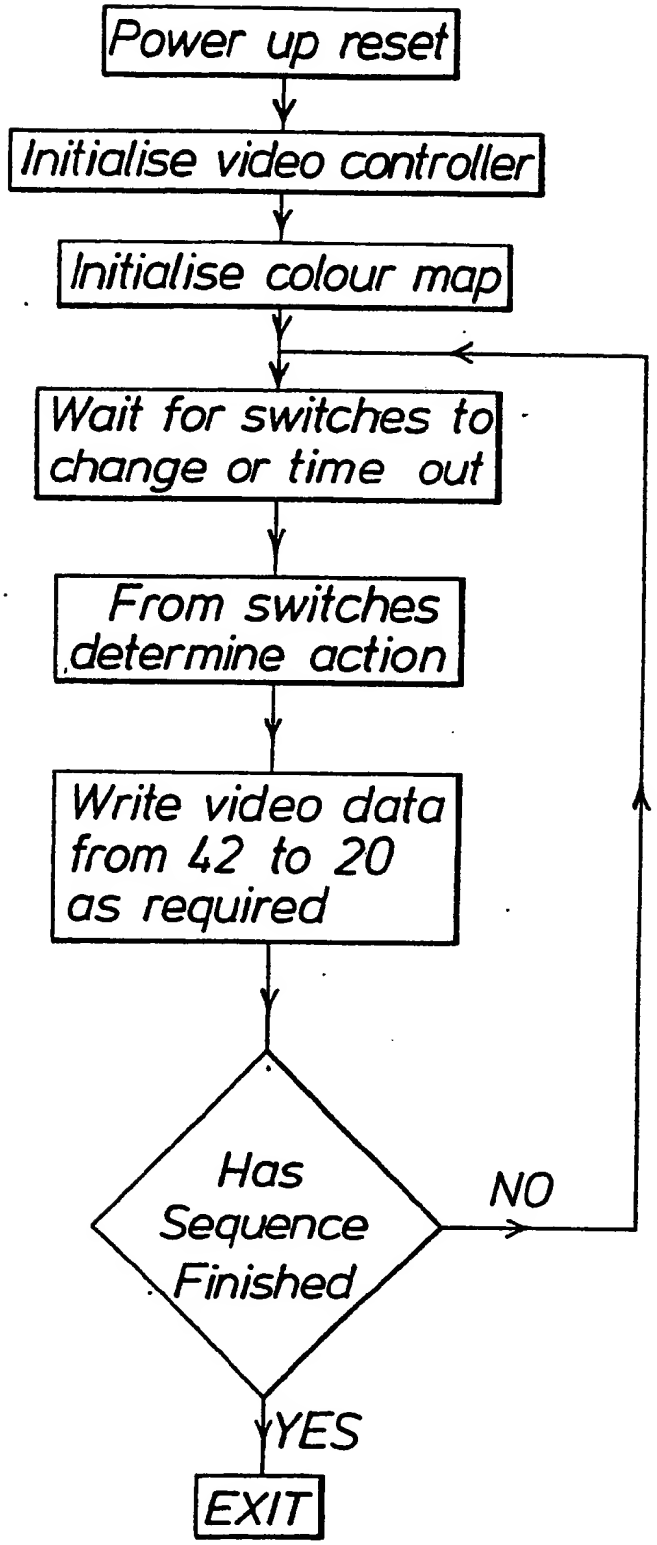


FIG. 4

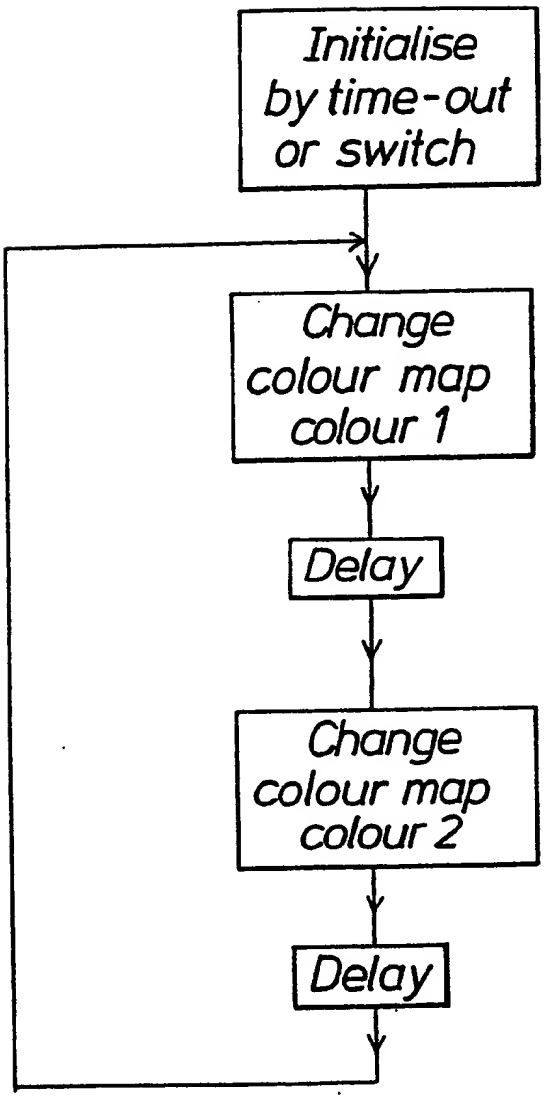


FIG.5

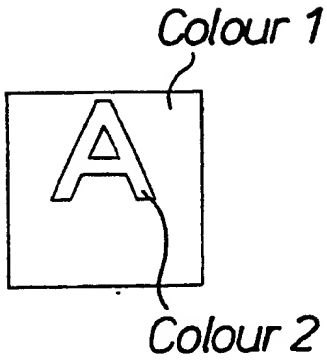


FIG.6

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